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# METHOD AND APPARATUS FOR ENHANCED TIMING LOOP FOR A PRML DATA CHANNEL

## Field of the Invention

The present invention relates generally to the data processing field, and more particularly, relates to a method and apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel in a direct access storage device (DASD).

## Description of the Related Art

Disk drive units often incorporating stacked, commonly rotated rigid magnetic disks are used for storage of data in magnetic form on the disk surfaces. Data is recorded in concentric, radially spaced data information tracks arrayed on the surfaces of the disks. Transducer heads driven in a path toward and away from the drive axis write data to the disks and read data from the disks. A partial-response maximum-likelihood (PRML) data detection channel advantageously is used to achieve high data density in writing and reading digital data on the disks. PRML data channels in DASD units are synchronous data detection channels where synchronous refers to the frequency and phase locking of the channel to the readback signal in order to detect the data properly.

Known data channels incorporate sophisticated timing loop algorithms to perform clock recovery during acquisition at the beginning of a read operation, and to keep the clock in synchronization during tracking for the remainder of the read operation. Problems with both the acquisition and

tracking timing loop algorithms have resulted as data channel detector improvements have allowed for lower operational signal to noise ratios (SNRs). Timing loop improvements in the noise robustness arena have not kept pace, causing performance problems at low SNR due to the timing loops.

A need exists for methods and apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel. It is desirable to provide such methods and apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel that provide improved performance in the presence of low SNR and that are effective, efficient and simple to implement.

**Summary of the Invention**

A principal object of the present invention is to provide improved methods and apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel. Other important objects of the present invention are to provide such methods and apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel substantially without negative effect and that overcome many of the disadvantages of prior art arrangements.

In brief, methods and apparatus for enhanced timing loop are provided for a partial-response maximum-likelihood (PRML) data channel in a direct access storage device (DASD). An acquisition timing circuit for generating an acquisition timing signal includes a plurality of compare functions for receiving and comparing consecutive input signal samples on an interleave with a threshold value. The acquisition timing circuit includes a majority rule voting function coupled to the plurality of compare functions for selecting a timing interleave.

Tracking timing circuitry for generating a timing error signal during a read operation includes a channel data detector. The channel data detector receives disk signal input samples and includes a multiple-state path memory. The tracking timing circuit includes a low latency detector receiving disk signal input samples. A selector function is coupled to an output of the

low latency detector and is coupled to the multiple-state path memory for selecting a state. The selector function utilizes the low latency detector output and selects the state of the path memory. The selector function provides a low latency output corresponding to the selected state. The low latency output is used for generating the timing error signal during a read operation.

**Brief Description of the Drawings**

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIG. 1 is a block diagram representation illustrating a PRML data channel for implementing methods for enhanced timing loop in accordance with the preferred embodiment;

FIGS. 2A and 2B are diagrams illustrating acquisition and tracking portions of a readback signal in the PRML data channel in accordance with the preferred embodiment;

FIG. 3 is a diagram illustrating an exemplary readback sync field signal used for implementing methods for enhanced timing loop in accordance with the preferred embodiment;

FIG. 4 is a block diagram illustrating a portion of a known acquisition timing circuit;

FIG. 5 is a block diagram illustrating an acquisition timing circuit in accordance with the preferred embodiment;

FIGS. 6 and 7 are block diagrams illustrating a tracking timing circuit in accordance with the preferred embodiment.

**Detailed Description of the Preferred Embodiments**

Having reference now to the drawings, in FIG. 1, there is shown a PRML data channel for implementing methods for enhanced timing loop in accordance with the preferred embodiment generally designated by the reference character 100. As shown in FIG. 1 in the PRML data channel 100, a read signal is applied to a variable gain amplifier (VGA) 102 and the amplified read signal is applied to an analog-to-digital converter (ADC) 104 that provides, for example, such as 64 possible 6-bit sampled values. The samples of the ADC 104 are applied to an equalizer 106, such as a 10 tap finite impulse response (FIR) digital filter. The filtered signal from the digital filter 106 is a class IV partial response (PR4) signal. The PR4 signal is input to two parallel paths. The filtered PR4 signal from the digital filter 106 is applied to a PRML detector 108, such as illustrated and described with respect to FIG. 7. The PRML detector 108 provides a detected data output. The filtered PR4 signal from the digital filter 106 and the samples of the ADC 104 are applied to a gain and timing control 110 of the preferred embodiment. Gain and timing control 110 of the preferred embodiment provides a timing control signal to a voltage controlled oscillator (VCO) 112 coupled to the ADC 104. Gain and timing control 110 provides a gain control signal to the VGA 102. Gain and timing control 110 of the preferred embodiment includes an acquisition timing circuit as illustrated and described with respect to FIG. 5 and tracking timing circuitry as illustrated and described with respect to FIGS. 6 and 7.

FIGS. 2A and 2B illustrates a readback operation 200 in the PRML data channel 100 including an acquisition portion or mode 202 and a tracking portion or mode 204 of in accordance with the preferred embodiment. When the data channel 100 begins a read operation, first the channel clock or VCO 112 must be synchronized to the input disk signal. As shown in FIG. 2B, the acquisition mode 202 includes a first phase lock mode 210 followed by a frequency and phase lock mode 212.

Referring also to FIG. 3, there is shown an exemplary readback sync field signal generally designated by the reference character 300 used for implementing methods for enhanced timing loop in accordance with the preferred embodiment. Sync field signal 300 is used for performing clock recovery during the acquisition mode 202. Sync field signal 300 is a sine wave with a frequency equal to 1/4 of the clock rate. At the start of

acquisition, the channel ADC 104 will be sampling the sync field signal 300 at an arbitrary and unknown phase, and at the end of acquisition, the channel ADC 104 will be sampling the sync field signal 300 on peaks 302 and zeros 304, as shown in FIG. 3. The zero samples 304 contain timing information, since the amplitude of these samples changes rapidly with any timing error. The peak samples 302 contain gain information, since the amplitude of these samples changes rapidly with any gain error. Thus, the acquisition algorithm uses two interleaves of samples, one for timing and the other for gain.

FIG. 4 illustrates a portion of a prior art acquisition timing circuit where the timing interleave is chosen based on a single sample $y_k$. An absolute value of the input sample is taken by an absolute value function ABS( ) and compared with a threshold value 0.5 by a compare function < to identify whether the sample $y_k$ is closer to a peak 302 or a zero 304. If the sample $y_k$ is closer to being a peak 302, the interleave for that sample is deemed the gain interleave and the other interleave becomes the timing interleave. If the sample $y_k$ is closer to being a zero 304, then the interleave for that sample is deemed the timing interleave and the other interleave becomes the gain interleave. In an ideal situation, the timing algorithm would only have to shift the phase of the clock 1/2 cycle due to this choice.

A significant problem in the current disk drive environment where the input signal is often noisy is the chance that the opposite timing interleave is selected. That is the single sample is deemed the timing interleave due to the noisy input signal when it is in fact the gain interleave. This requires the timing algorithm to shift the phase of the clock a full cycle, which takes longer than the time allotted so that acquisition fails.

In accordance with features of the preferred embodiment, an enhanced acquisition timing circuit as illustrated and described with respect to FIG. 5 provides significantly improved robustness over the prior art arrangements, such as shown in FIG. 4. The enhanced acquisition timing algorithm of the preferred embodiment uses multiple consecutive samples on an interleave, such as three consecutive samples on an interleave, determining whether each sample is closer to a peak 302 or a zero 304. Then majority rule voting, such as a two out of three voting scheme, is used

to determine the timing interleave.

FIG. 5 illustrates an acquisition timing circuit generally designated by the reference character 500 in accordance with the preferred embodiment. Acquisition timing circuit 500 is shown in simplified form sufficient for an understanding of the invention. Acquisition timing circuit 500 receives multiple consecutive samples on an interleave $y_k$, $y_{k-2}$, and $y_{k-4}$ and an absolute value of each input sample is taken by a respective absolute value function ABS( ) 502, 504, 506. Each absolute sample values is compared with a threshold value 0.5 by a respective compare function 508, 510, 512 to identify whether each sample $y_k$, $y_{k-2}$, and $y_{k-4}$ is closer to a peak 302 or a zero 304. The outputs of the compare functions 508, 510, 512 are applied to a majority rule voting function 514, such as two out of three voting function as shown, selecting a timing interleave. The output of majority rule voting function 514 is applied to an input of a multiplexer 520 having its output coupled to a latch 522. A timing interleave output of the latch is connected to a second input of the multiplexer 520. Acquisition timing circuit 500 significantly improves robustness of the acquisition timing algorithm in the presences of noise with a small increase in the length of acquisition for receiving the multiple consecutive samples on an interleave $y_k$, $y_{k-2}$, and $y_{k-4}$. However, the increased length of acquisition for the acquisition timing circuit 500 is not nearly as much as allowing for a full cycle phase correction as may be required for the conventional timing algorithm.

FIGS. 6 and 7 illustrate tracking timing circuitry generally designated by the respective reference characters 600 and 700 in accordance with the preferred embodiment. Tracking timing circuitry 600 and 700 is shown in simplified form sufficient for an understanding of the invention. While the data channel 100 is performing a read operation, the channel clock must be synchronized to the input read signal. To accomplish this, timing error information shown as $Terr_k$ in FIG. 7 must be generated based on the data being read. This timing error signal $Terr_k$ is applied by the tracking timing algorithm for applying corrections to the VCO 112 to keep the clock in synchronization during tracking for the remainder of the read operation.

In accordance with features of the preferred embodiment, the enhanced tracking timing circuitry 600 and 700 minimizes the latency in

generating the timing error signal $Terr_K$ for optimum timing loop performance. In conventional arrangements, the timing error is determined using the output of the data detector in the PRML data channel. In recent data channels, the data detector has become extremely sophisticated with capability of accurately reading data at very poor signal to noise ratios. One of the problems with such sophistication of the data detector is an extremely long latency, or delay from samples in to detected data out. This long latency makes the conventional tracking timing arrangements that use the output of the data detector unacceptably poor. Enhanced tracking timing circuitry 600 and 700 solves this problem.

Enhanced tracking timing circuitry 600 includes the data detector 108, such as a 16-state detector including a matched filter 602, an add compare select 604 and a multiple-state path memory 606. Data detector 108 receives an input $y_K$ from the FIR filter 106 and provides an output $a_{K-N}$ at the output of path memory 606. A lower latency detector 608, such as 4-state PR4 Viterbi detector receives the input $y_K$ and provides a low latency output $a_{K-L}$. The output $a_{K-L}$ of detector 608 is unacceptable to generate timing error because the PR4 detector's error rate is extremely poor at current high user bit densities. The output $a_{K-L}$ of detector 608 is applied to a 16-way selector 610. The 16-way selector 610 is coupled to the path memory 606 of the data detector 108. The 16-way selector 610 utilizes the output $a_{K-L}$ of detector 608 to selects which state in the path memory 606 to choose. The16-way selector 610 to pull the data out from an early or low latency state in the path memory 606 of the detector 108 applies a simplified best metric selection algorithm. Operation of the 16-way selector 610 significantly reduces the latency without a severe error rate penalty. The 16-way selector 610 uses the low latency PR4 Viterbi detector output to select the low latency state of the path memory 606 for providing an output $a_{K-M}$, where $L < M < N$. The output $a_{K-M}$ is used for generating a timing error in accordance with the preferred embodiment.

Referring to FIG. 7, the timing error $Terr_K$ in accordance with the preferred embodiment is generated by applying the input $y_K$ from the FIR filter 106 to an adder 702. The output $a_{K-M}$ of the 16-way selector 610 is applied to a convert-to-estimated-sample function 704 for generating an estimated sample output $\hat{y}_K$. Convert-to-estimated-sample function 704

applies the estimated sample output $\hat{y}_K$ to the adder 702 where the estimated sample output $\hat{y}_K$ is subtracted from the input $y_K$ by adder 702 to generate the timing error $Terr_K$.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.